of the graph to ensure correct timing operation of the circuit. Building of such a graph for both gate-level netlists and transistor-level netlists is known in the prior art.

The next step is to conduct statistical timing analysis of the electrical circuit, box 230, which is preferably, but not necessarily, conducted as taught in the co-pending application: C. Visweswariah, "System and Method for Statistical Timing Analysis of Digital Circuits," ~~Docket number YOR92003-0403US1,~~ U.S. Patent Application Number 10/666,470 ~~(to be assigned)~~ on 09/1~~8~~9/03. During the statistical timing analysis, arrival and required arrival tightness probabilities on each edge of the timing graph are saved for future use.

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Next, in box 240, the tightness probabilities of all end points are determined by an inventive method that will be described in detail later. This is an optional step. If overall criticality probabilities are desired on a per-end-point basis, this step can be skipped. However, if overall criticality probabilities are desired for the entire electrical circuit, then this step is required. Next, in box 250, a backward propagation is carried out to determine the criticality probabilities of each edge and node of the timing graph by an inventive method that will be explained later. Finally, in box 260, timing reports are produced of the type in boxes 150 and 160 of Figure 1, either in a file or as return values of a function call. These reported values can include probabilities of individual timing tests being met; probabilities of primary outputs meeting their required arrival times; arrival tightness probabilities, required arrival tightness probabilities; node criticality probabilities; edge criticality probabilities; path criticality probabilities; a list of paths